

1st Workshop on High Performance FPGA/Reconfigurable Computing

at 15th IEEE International Conference on High Performance Computing (HiPC)

Bangalore, India

December 17, 2008

<http://www.hipc.org>

CALL FOR EXTENDED ABSTRACTS

WORKSHOP IMPORTANT DATES

September 1, 2008	Extended Abstract Submissions
October 1, 2008	Accept/Reject Decisions
November 1, 2008	Camera-Ready Papers Due
December 17, 2008	Workshop

WORKSHOP CHAIR*

Tirumale Ramesh, The Boeing Company, USA

WORKSHOP DEPUTY CHAIR*

Venkat Ramana, Hinditron-CRAY, India

WORKSHOP PROGRAM COMMITTEE**

Includes Chair and Deputy Chair*

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John Meier, The Boeing Company, USA

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Brent Nelson, Brigham Young University, USA

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** More representations to be added

TCPP Organization Chair

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Continued research and development in both embedded and high-end computing are addressing the potentials of conventional and unconventional reconfigurable architectures and how it is implemented. There is a new breed of application interests in these areas that utilizes both fine-grain and coarse-grain parallelism with a vast potential for adaptation of reconfigurable processing elements. Reconfigurable/FPGA solutions are showing promises of value metrics for industries with quick time-to-market for products, reduced design cycle time, reduced system costs & power usage, and enhancing system fault-tolerance.

The half-day workshop will bring together architects, designers, tools and applications developers of FPGA/Reconfigurable Computing to provide a forum for presenting the state-of-the-art in Reconfigurable/FPGA platforms, solutions and technologies, and for exchanging their experiences.

Prospective Authors should submit extended abstracts (3-4 pages in length) on their original work on topics of interest include, but not limited to: innovative and disruptive reconfigurable architectural paradigms, models, algorithms, tools and methods for reconfigurable computing, reconfigurable hardware-software co-design, evolvable and dynamic reconfigurable hardware, reconfigurable applications and education. The workshop is much interested in receiving submissions from diversified areas of reconfigurable computing applications, but not limited to: security, cognitive processing, bio-inspired reconfigurable computing fabric, reconfigurable DSP and network processing. Industrial applications focus in space & aerospace, defense, automobile, network, life and health sciences are much encouraged. Extended abstracts shall be submitted by **September 1, 2008** via email to Tirumale Ramesh, Workshop chair, at tirumale.k.ramesh@boeing.com. All extended abstract submitted to the workshop will be peer-reviewed by at least three members of the program committee and authors will be notified of acceptance/rejection decisions in a timely manner. The workshop advance program will be posted on the workshop's website well in advance of the workshop. Camera-Ready papers of accepted extended abstracts should be submitted by **November 1, 2008**.

MANUSCRIPT GUIDELINES FOR CAMERA-READY PAPERS

Submitted manuscripts should be structured as technical papers and may not exceed 6 letter size (8.5 x 11) pages including figures, tables and references. Formatting requirements are 12-point font size, single spaced or higher, with margins of at least 1 inch on each of the four sides. Submissions not conforming to these guidelines may be returned. Authors should submit the manuscript in PDF format and make sure that the file will print on a printer that uses letter size (8.5 x 11) paper. The official language of the meeting is English. Subject to the availability of sufficient number of peer-reviewed papers, all workshop camera-ready papers will be published as a separate CDROM Proceedings by HiPC. There will be NO hard copy proceedings for the workshops published by HiPC.

Planned Workshop Technical Program

The workshop technical program will consist of 1-2 invited papers and 6 peer reviewed contributed papers with representative contributions from industry, academia and government organizations generally addressing the impact of high performance FPGA/Reconfigurable computing on current high performance computing paradigm. All workshop presenters and attendees are required to be registered for HiPC 08. The workshop is organized by the IEEE Computer Society Technical Committee on Parallel Processing (TCPP) Sub-committee on Reconfigurable Systems and Architectures.

Sponsored by: IEEE Computer Society Technical Committee on Parallel Processing, ACM SIGARCH, European Association for Theoretical Computer Science, IFIP Working Group on Concurrent Systems, National Association of Software and Service Companies, and Manufacturers' Association for Information Technology.

